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FIG. 1A

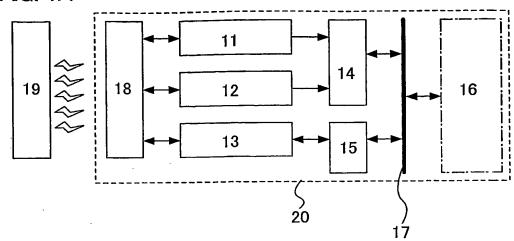
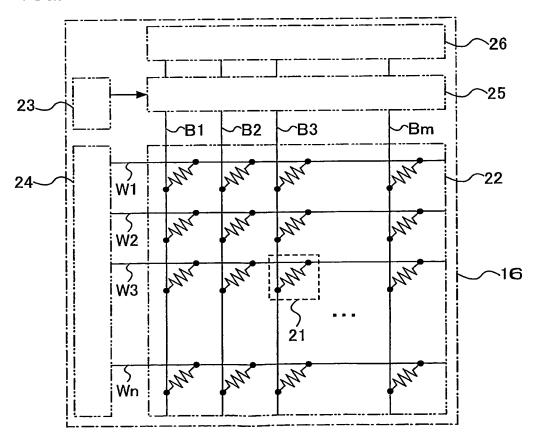
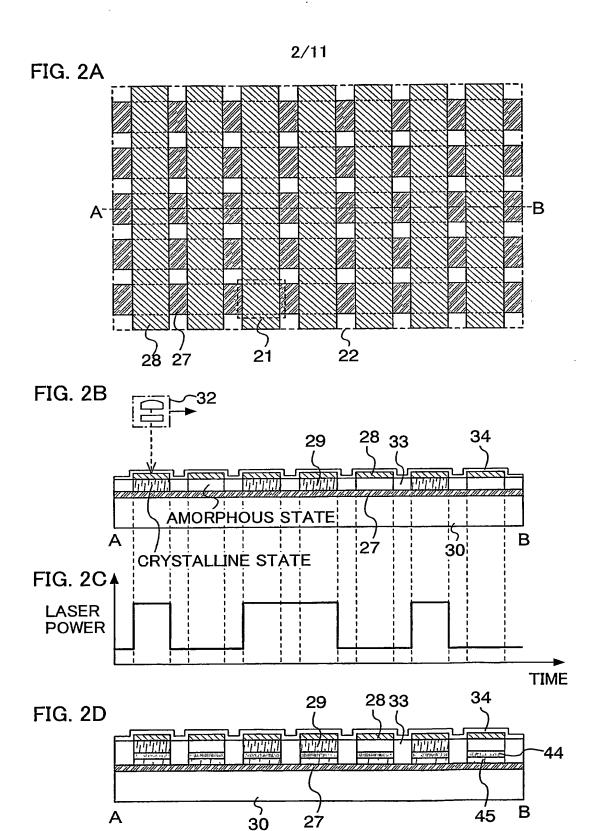
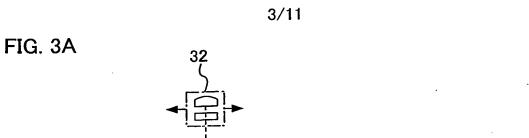


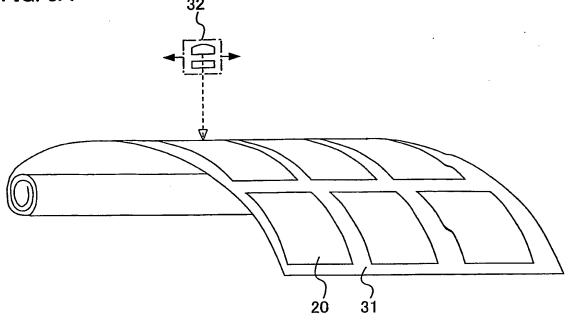
FIG. 1B

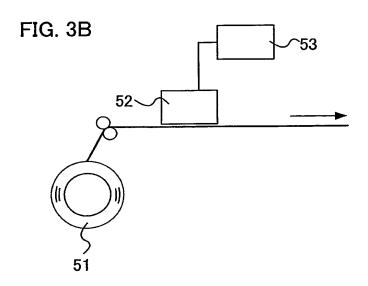




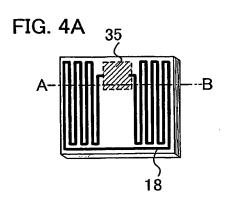
PCT/JP2005/006713 WO 2005/096380

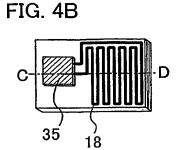


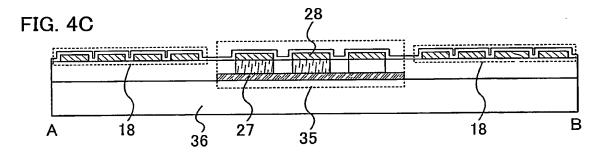


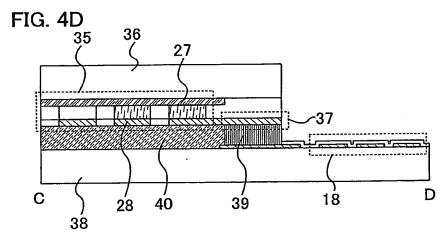


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FIG. 5A

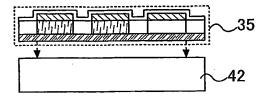
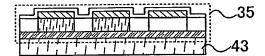
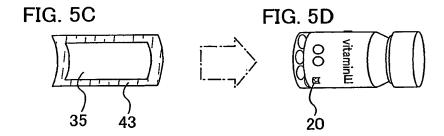
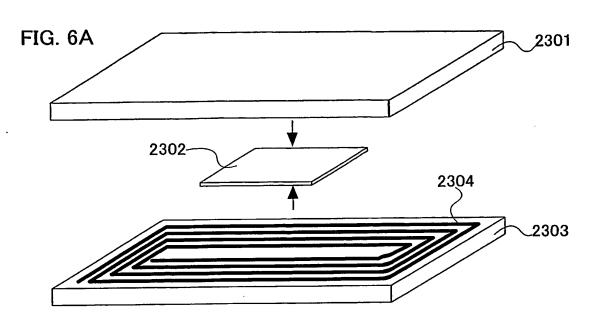
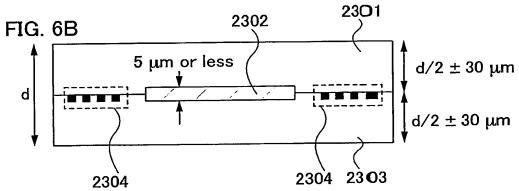


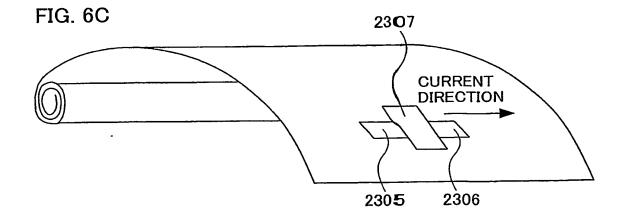
FIG. 5B



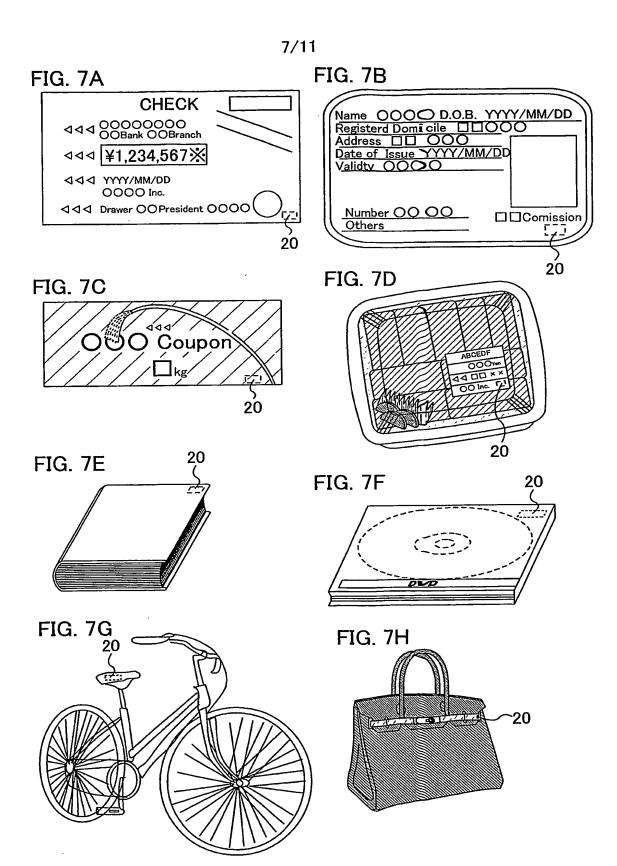


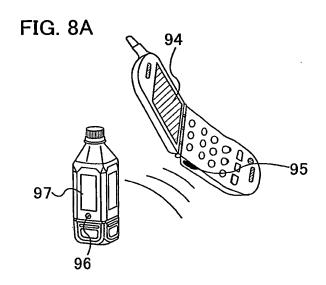


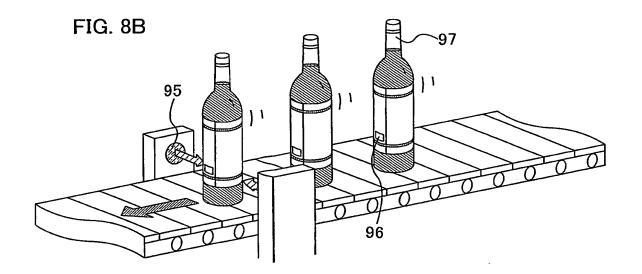




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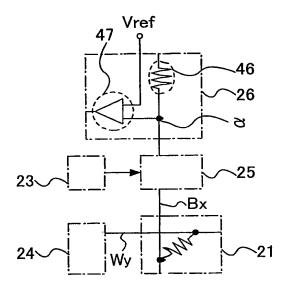
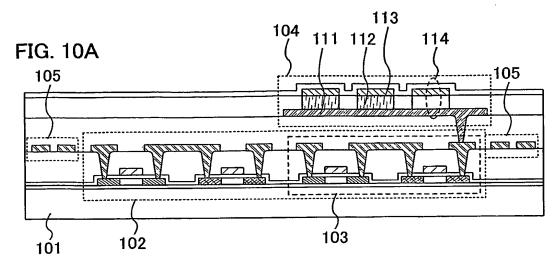
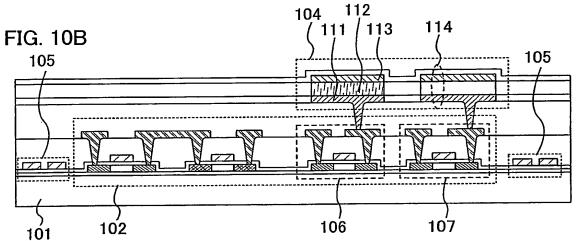


FIG. 9

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EXPLANATION OF REFERENCE

generating circuit, 13: data 12: clock circuit, 11: power source demodulation/modulation circuit, 14: control circuit, 15: interface circuit, 16: memory, 17: data bus, 18: antenna, 19: reader/writer, 20: semiconductor device, 21: memory cell, 22: memory cell array, 23: decoder, 24: decoder, 25: selector, 26: read/write circuit, 27: first conductive layer, 28: second conductive layer, 29: phase change layer, 30: substrate, 31: flexible substrate, 32: laser light irradiating means, 33: insulating layer, 34: insulating layer, 35: element group, 36: substrate, 37: terminal portion, 38: substrate, 40: resin, 42: substrate, 43: flexible substrate, 44: semiconductor layer, 45: semiconductor layer, 46: resistor, 47: sense amplifier, 51: roll, 52: heating means, 53: control means, 94: display portion, 95: reader/writer, 96: wireless tag, 97: product, 1 01: substrate, 102: element group, 103: CMOS circuit, 104: phase change memory, 1 05: antenna, 106: transistor, 107: transistor, 111: conductive layer, 112: phase change layer, 113: conductive layer, 114: memory element, 2301: protective layer, 2302: element group, 2303: protective layer, 2304: antenna, 2305: electrode, 2306: electrode, 2307: electrode.